Application No.: 10/743,934 Docket No.: 29936/39901

AMENDMENTS TO THE SPECIFICATION

Please amend paragraph [0001] as follows:

Technical Field of the Invention

[0001] The present invention relates to a data input/output buffer and a semiconductor memory device using the same, and more specifically, to a \underline{A} data input/output buffer that can exactly sense an input signal even if the signal is inputted as a low voltage due to a drop in a threshold voltage, and a semiconductor memory device using the same are disclosed.

Please <u>amend</u> paragraphs [0005] – [0007] as follows:

SUMMARY OF THE INVENTION DISCLOSURE

[0005] The present invention relates to a A data input/output buffer and a semiconductor memory device using the same are disclosed, which can improve reliability of a circuit by exactly determining the level of a data signal even if the data signal is inputted as a level that is lowered as much as a threshold voltage, in such a manner that a transistor of a switching means or a logical element out of devices constituting the data input/output buffer, to which the data signal is inputted most rapidly is implemented using a low voltage-driven device whose threshold voltage is low.

[0006] According to one embodiment of the present invention, there is provided a data input/output buffer, including a plurality of switching elements and logical elements, wherein an NMOS transistor of a switching element driven according to a data signal inputted from a peripheral circuit or a logical element to which the data signal is inputted, of the plurality of the switching elements or the plurality of the logical elements, is a low voltage-driven NMOS transistor.

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[0007] According to another embodiment of the present invention, there is provided a data input/output buffer, including a first logical element driven according to a data signal inputted from a peripheral circuit, the first logical element having a PMOS transistor and a low voltage-driven NMOS transistor; and a second logical element for latching an output signal of the first logical element.

Please <u>amend</u> paragraph [0009] as follows:

[0009] According to one embodiment of the present invention, there is provided a semiconductor memory device, including a memory cell array; a row decoder for selecting a given page of the memory cell array according to a row address signal; a page buffer for storing data stored at the page selected by the row decoder; a column decoder for generating a bit line select signal according to a column address signal; a column multiplexer for selecting any one of the data stored at the page buffer according to the bit line select signal; and a data input/output buffer for storing the data selected by the column multiplexer and transferring the data to a data line, wherein a device driven by the data is a low voltage-driven NMOS transistor.

Please amend paragraph [0012] as follows:

[0012] Fig. 1 is a block diagram illustrating the construction and the operation of a semiconductor memory device using a data input/output buffer according to an embodiment of the present invention;

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Please amend paragraph [0015] as follows:

[0015] Now, the preferred embodiments according to the present invention will be described with reference to the accompanying drawings. Since preferred embodiments are provided for the purpose that the ordinary skilled in the art are able to understand the present invention, they may be modified in various manners and the scope of the present invention is not limited by the preferred embodiments described later.